High Linearity, Low Noise IF transmitter for WCDMA Application

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Abstract — **An integrated IF transmitter with on-chip synthesizer for W-CDMA application is presented. It was designed to comply with UMTS standard on a low cost application board. The 5-MHz ACLR is better than -60 dBc while output noise at maximum and minimum gain setting is -147 dBm/Hz and -167 dBm/Hz respectively, which is the minimum reported to date. Furthermore, the gain control curve linearity exceeds 3GPP requirements with a dynamic range higher than 80 dB.**

I. INTRODUCTION

The third generation cellular systems, called Universal Mobile Telecommunications Systems (UMTS), are going to enter the market with phones able to manage different kinds of multimedia data and applications. The access technique used for UMTS is the Wideband Code Division Multiple Access (W-CDMA), which allows high transfer rate. Due to the stringent performance required by 3GPP standard, double conversion architecture is usually used for the transmitter. Indeed, double conversion has better performance in terms of noise and spurious emission and guarantees accurate I/Q paths. Moreover, thanks to the inherent isolation, it allows high power control range to be achieved. One of the key blocks of such an architecture is the IF transmitter which strongly influences the linearity and noise performance of the whole transmission chain. Minimizing noise produced by the IF transmitter has different benefits on the overall transmission chain performance. Indeed, at high gain setting, low value for out-of-band noise allows SAW filter requirements to be relaxed; on the other hand, at low gain setting, low amount of output noise improves the EVM (Error Vector Magnitude) of the whole transmission chain, and relaxes the specifications of other TX blocks. The same concept applies for linearity where the maximization of Adjacent Channel Leakage Ratio (ACLR) on IF transmitter saves current consumption and reduces the cost of the RF up-converter, PA and external filters. Moreover a very linear gain control is generally required to simplify complexity of base-band control circuit and, at the same time, to meet the stringent 3GPP requirements on the power control accuracy [1].

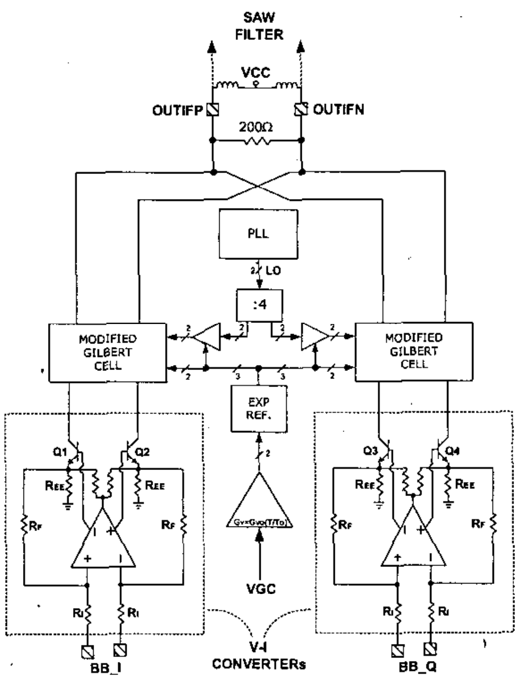

Fig. 1. Transmitter Simplified Diagram

The proposed integrated IF transmitter with on-chip synthesizer for W-CDMA application represents the state-of-the-art of monolithic IF transmitters as high linearity and low noise performance are simultaneously achieved. It was designed to comply with the UMTS standard on a low cost application board. The device was implemented with STMicroelectronics SiGe BICMOS process with 45-GHz bipolar and 0.35-um CMOS devices. The IC complies UMTS specifications with supply voltage between 2.7 V and 3 V and ambient temperatures between –20 and 75 Celsius degrees.

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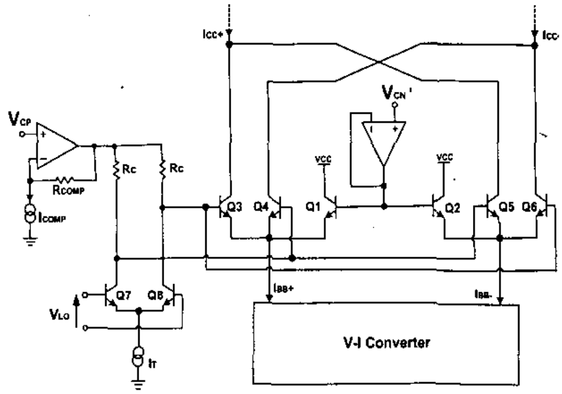

Fig. 2. Modified Gilbert Cell

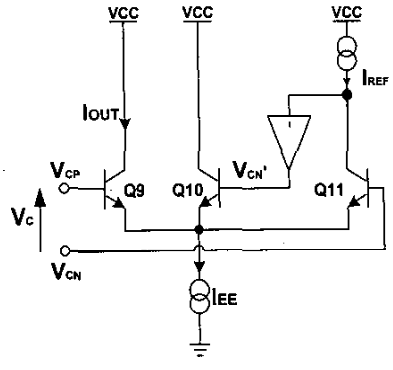

Fig. 3. Exponential Reference Circuit

II. CIRCUIT DESCRIPTION

Fig. 1 shows the block diagram of the IF transmitter. The circuit converts the I/Q signals coming from the base-band chip into a 380-MHz modulated signal with gain adjustable according to a suitable control voltage (VGC). I/Q base-band signals are processed separately by the relative section and they are added after up-conversion operation. Each section is composed of a voltage to current converter and a modified Gilbert cell. Thanks to the feedback realized by a 70-MHz gain-bandwidth OpAmp, the linearity of the transconductors is considerably boosted by the loop gain, providing high IM3 performance even with low voltage drop across the degeneration resistors (R_{EE}). Once the degeneration resistors are chosen according to the load and gain constraints, the bias current is set to limit IM3 degradation of the modified Gilbert cell.

Special care was put to minimize the LO injection which is due to different phenomena depending on the selected gain value. Indeed, at high gain, it is mainly due to the base-band DC offset, while, at low gain, it is limited by the parasitic coupling between the internal 380-MHz LO signal and the output port. Therefore, in order to minimize the transconductor DC offset, a very-low-offset OpAmp was designed and the layout of feedback resistors was arranged to minimize mismatches. The measured LO-rejection, for gain higher than -50 dB, is at least -30 dBc without any external tuning. Moreover the layout design was optimized in order to improve the internal isolation. A value better than 80 dB was achieved for this parameter leading to an LO injection in the output port lower than -90 dBm for gain value lower than -50 dB.

The core structure of the transmitter is the modified Gilbert cell, whose simplified schematic is presented in Fig. 2 [2]. Basically it consists of a traditional Gilbert cell Q3-Q6 on which two transistors Q1-Q2 are added.

During each LO phase either Q3, Q6 or Q4, Q5 are active, so that each pair, made up of these transistors and Q1 (or Q2), performs a current steering between load and supply voltage depending on the voltage between nodes V_{CP} and V_{CN}'. As clarified below, the differential signal between such nodes is the pre-distorted signal extracted from the gain control voltage V_C.

In each LO phase the base voltages of active transistors are connected to V_{CP} through a R_C resistor and the OpAmp buffer. The voltage $I_{COMP} \cdot R_{COMP}$ compensates for the voltage drop across the R_C resistors due to the base currents of Q3-Q6. A special circuit generates the current I_{COMP} as scaled replica of such a base currents.

In this way the variable gain amplification is performed directly in the modulator and the whole structure can be seen as a Variable Gain Modulator (VGM). Compared to the traditional two-stage approach this architecture achieves better linearity and noise performance with the same current consumption. Furthermore, it allows to avoid the third-harmonic low-pass filter usually introduced between the modulator and Variable Gain Amplifier (VGA) to boost the VGA linearity performance, with consequent benefit of the area occupation [3].

The accurate linear-in-dB gain curve is achieved by a suitable pre-distortion of the control voltage operated for both I/Q sections by the exponential-reference circuit. The simplified schema of such a circuit is shown in Fig. 3. For the sake of simplicity it is useful to assume that transistors Q9 and Q11 have the same emitter area. The loop amplifier acts on transistor Q10 in order to ensure that the collector current of the transistor Q11 is exactly equal to the constant current I_{REF}. As a consequence, the V_{BE11} is maintained constant too. So if the control voltage V_C is zero the output current I_{OUT} is equal to the reference current I_{REF}; otherwise the control voltage drop V_C is directly added to the quiescent value of V_{BE9}.

So, for the basic transistor law, it means that the output current I_{OUT} depends on the control voltage V_C by a pure exponential law, according to the following expression.

$$I_{OUT} = I_{REF} \cdot \exp\left(\frac{V_C}{V_T}\right) \quad (1)$$

The pre-distorted voltages V_{CP} and V_{CN}' (see Fig. 3) are then applied to the modified Gilbert cell in order to replicate the same law. Because the transfer function of such a circuit is proportional to $\exp(V_C/V_T)$, a temperature compensation is realized by a further stage having a gain Proportional To Absolute Temperature (PTAT). A translinear circuit, whose gain varies according to the following expression, performs the PTAT gain.

$$A_V(T) = \frac{2Rc}{R_E}\frac{I_{PTAT}}{I_{GAP}} \quad (2)$$

I_{PTAT} and I_{GAP} are a PTAT and a band-gap derived current respectively.

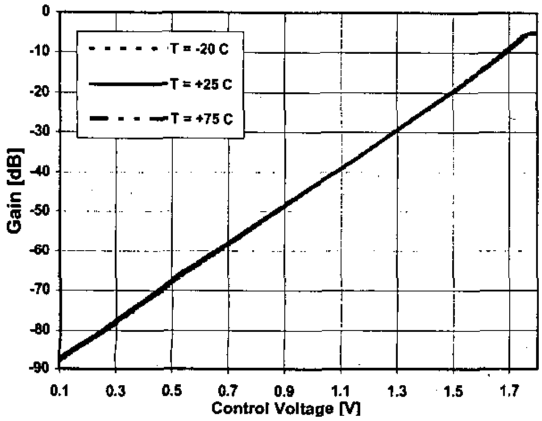

Fig. 4. Gain curve vs. control voltage

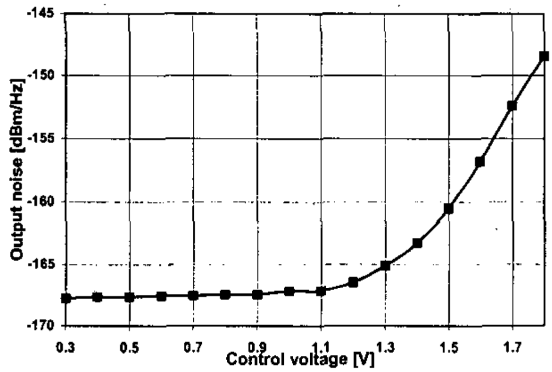

Fig. 5. Output noise referred to 200-Ω load

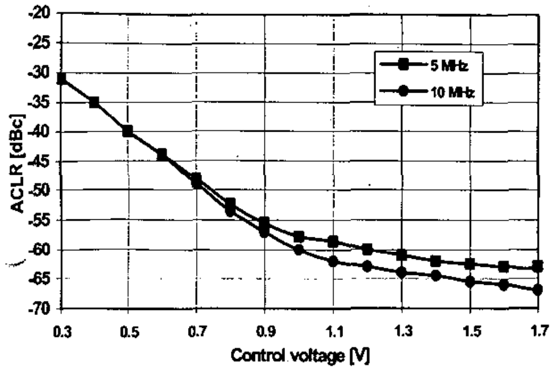

Fig. 6. ACLR @ 5MHz and 10 MHz

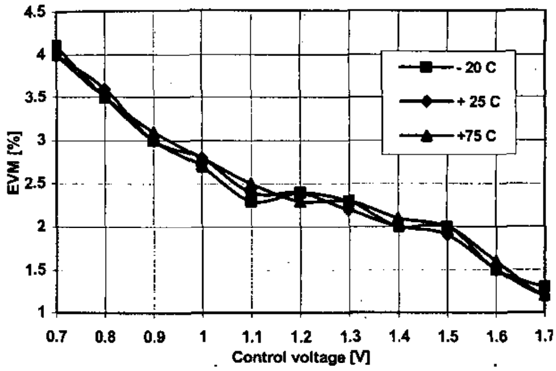

Fig. 7. Error Vector Magnitude

An integrated integer PLL using an auxiliary VCO operating at 1520 MHz and an external loop filter provides the high frequency local oscillator signal. A divider by four generates the accurate quadrature local oscillator signals for the up-conversion operation, independently from the duty cycle of VCO output signal.

The transmitter output matches a 200Ω-load that is the usual input impedance for IF SAW filters available on the market. Two choke inductors are connected between the open-collector outputs and power supply (V_{CC}). They provide large swing and broadband frequency response.

I/Q inputs can be either DC or AC coupled to the base-band chip.

III. MEASUREMENTS

It is important to remark that the VGM is particularly suitable to be used as an attenuator since input and output signals have different frequencies and then a good isolation is achieved. The measured gain as a function of the control voltage in the range 0.1 V to 1.8 V is shown in Fig. 4. Thanks to the predistortion operated by the VGM exponential reference the linearity of the gain curve exceeds 3GPP requirement in the temperature range between -20 and 75 Celsius degrees with a dynamic range higher than 80dB. As shown in Fig. 5, the out-of-band noise at maximum and minimum gain setting is -147 dBm/Hz and -167 dBm/Hz respectively, which is the best result reported in literature to date.

The ACLR at low gain is mainly due to the noise at the adjacent channel, which is minimized in the current design. So both the EVM and low-gain ACLR take benefit of such a low noise. Fig. 6 shows ACLR at 5 MHz and at 10 MHz. The high linearity of the device is demonstrated by the measurement of ACLR at maximum gain setting. In such a condition ACLR is -63 dBc and -67 dBc at 5 MHz and at 10 MHz respectively. The EVM at different temperatures in the 0.7 V-1.7 V control voltage range is shown in Fig. 7. The current consumption of the whole IC is 49 mA, of which 7.5 mA is the current consumption of the PLL blocks. The Table I resumes the main device performance.

IV. Conclusion

An IF transmitter with on chip PLL, suitable for low-cost double-conversion TX application, has been presented. Indeed, thanks to the very low noise and high linearity, it gives negligible contribution to the total EVM and ACPR TX chain budget. As an immediate consequence cheaper filters can be used on the application board and, at the same time, the requirements of RF TX blocks are heavily relaxed with advantage of the overall current consumption. These performances have been accomplished by the particular architecture chosen for the modulator (VGM), which performs both the modulation and variable gain amplification, sharing the same bias current for the two functional blocks without penalizing the dynamic range.

TABLE I
SUMMARY OF THE PERFORMANCE

Parameter	Gain value	Measurement
Gain (dB)	--	-87 ÷ -4
Output noise (dBm/Hz)	Max	-148
	Min	-167
ACLR @ 5 MHz (dBc)	-10dB	-63
	-78dB	-31
ACLR @ 10 MHz (dBc)	-10dB	-67
	-78dB	-31
LO carrier leakage (dBc)	> -50 dB	< -30
LO carrier leakage (dBm)	< -50 dB	-90
EVM (%)	> -55 dB	< 3.5
Overall Supply Current (mA)	49	

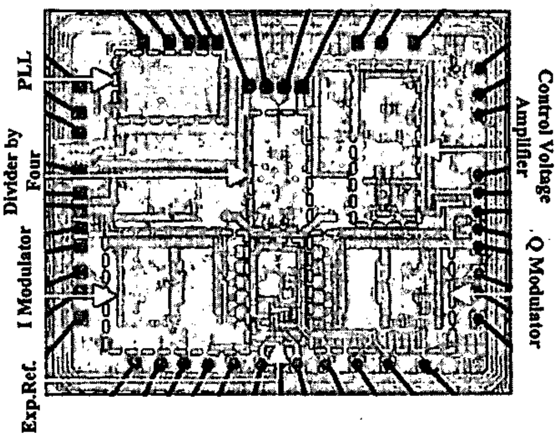

Fig. 8. Chip Photo

Moreover since that input and output signals of VGM have different frequency, the isolation is almost unlimited and consequently a very high dynamic gain can be achieved. In the current design a dynamic range higher than 80 dB is measured.

The device has been characterized in the temperature range between -20 and 75 Celsius degrees and it fully complies 3GPP requirements. The IC die size is 2.14 x 2.6 mm^2 and was assembled in a 36-pin leadless package. The chip photo is shown in Fig. 8.

Acknowledgement

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